Julien VILLEMEJANE - 1A2S

Un Monde Tout Numérique

EITI 2016-2017

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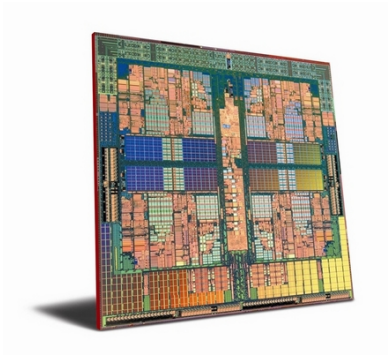
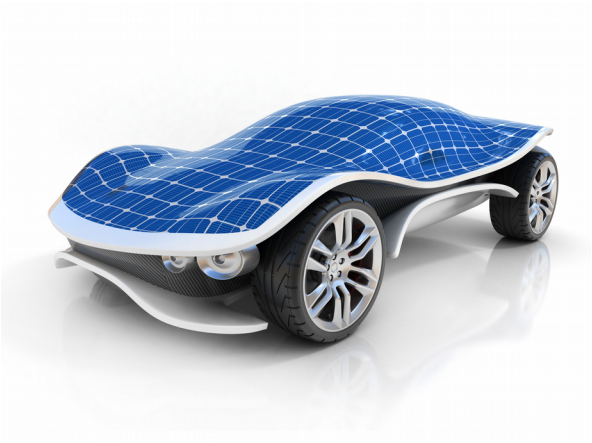
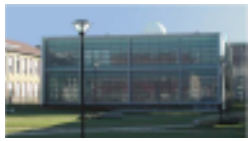
Un Monde Tout Numérique





Paris-Saclay



Saint-Étienne

Bordeaux

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1981 - IBM PC / 4,77 MHz / 16 à 256 Ko - 1800 $

1985

Un Monde Tout Numérique

1984 - Apple Macintosch / 8 MHz - 16 bits / 128 Ko

1973 - Micral - R2E / France

Un monde tout numérique

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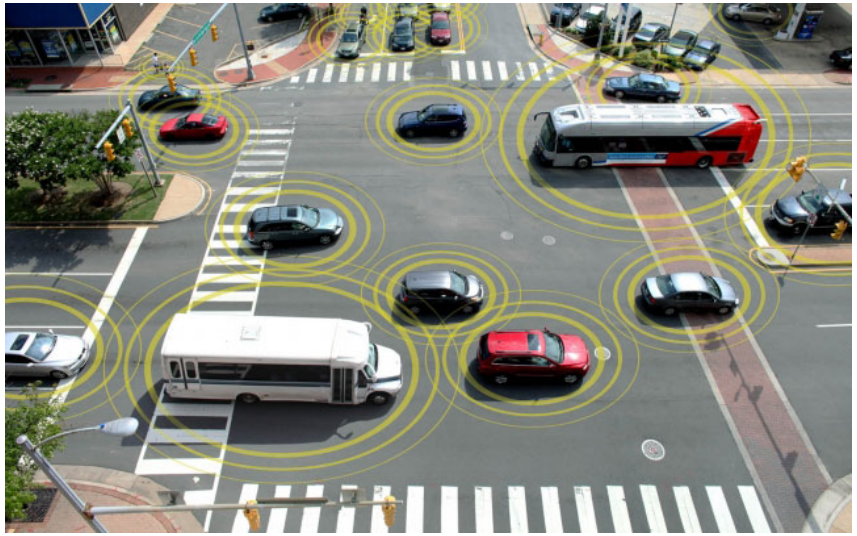
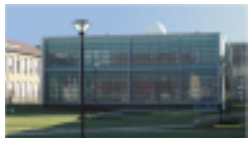
Autour de nous



Paris-Saclay



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Un monde tout numérique

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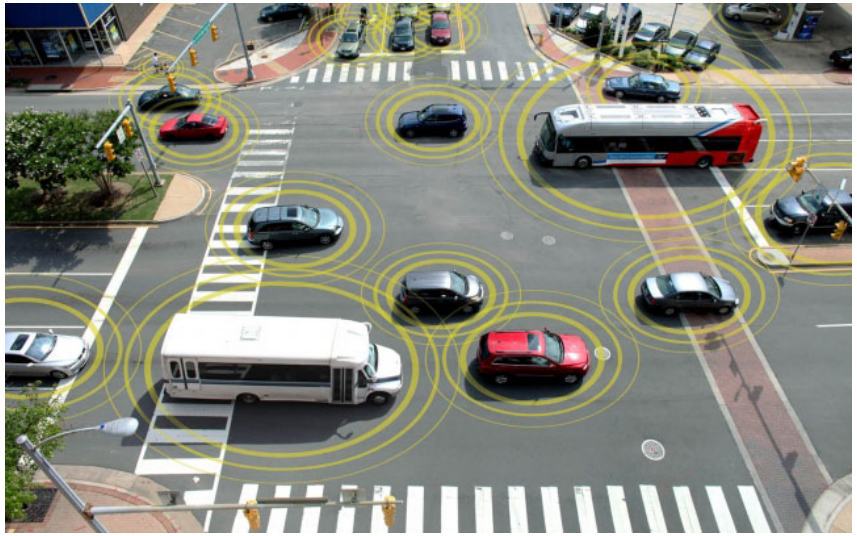


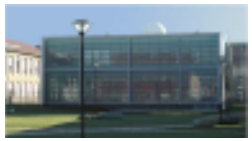
Un monde connecté

- *Des tonnes de données numériques transmises*
  - *STOCKAGE*

Un monde automatisé

- *Des traitements numériques en temps réel*
  - *RAPIDES*
  - *RECONFIGURABLES*
  - *AUTO-DIAGNOSTIC*

Paris-Saclay



Saint-Étienne

Bordeaux

Un monde tout numérique

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Des EB de données à traiter

Google

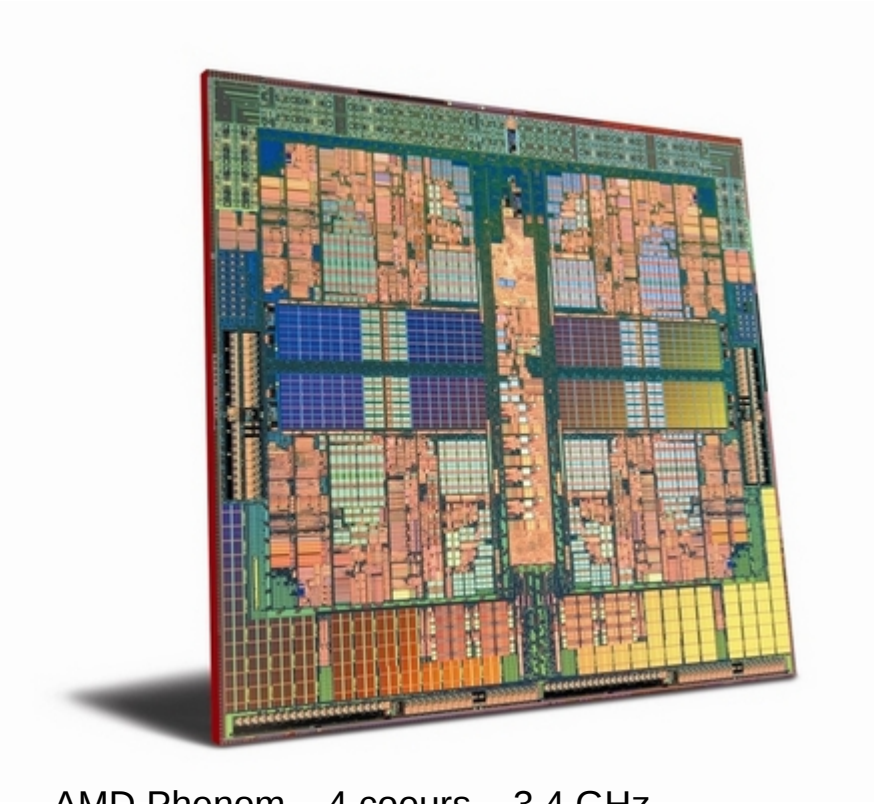
- *900.000 serveurs dans le monde*
- *260 MW de puissance*
  - *200.000 foyers environ*

FaceBook

- *750 TB / jour*
- *Capacité de 100 PB*
- *7 PB de photos / mois*

TB : TeraOctets 10^{12} ,
PB : PetaOctets 10^{15} ,
EB : ExaOctets 10^{18}

Traitement numérique

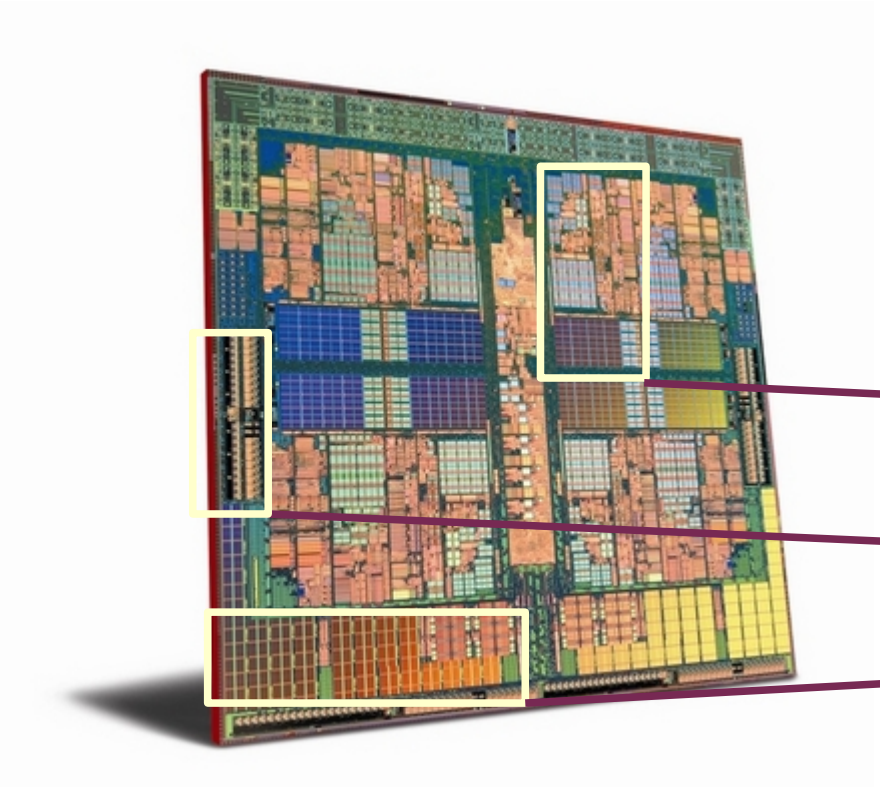


AMD Phenom – 4 coeurs – 3.4 GHz

Processeur

- *Exécution d'**instructions** de **manière séquentielle***
- ***Unités de calculs** précablées*

Traitement numérique



AMD Phenom – 4 coeurs – 3.4 GHz – 2 milliards

Processeur

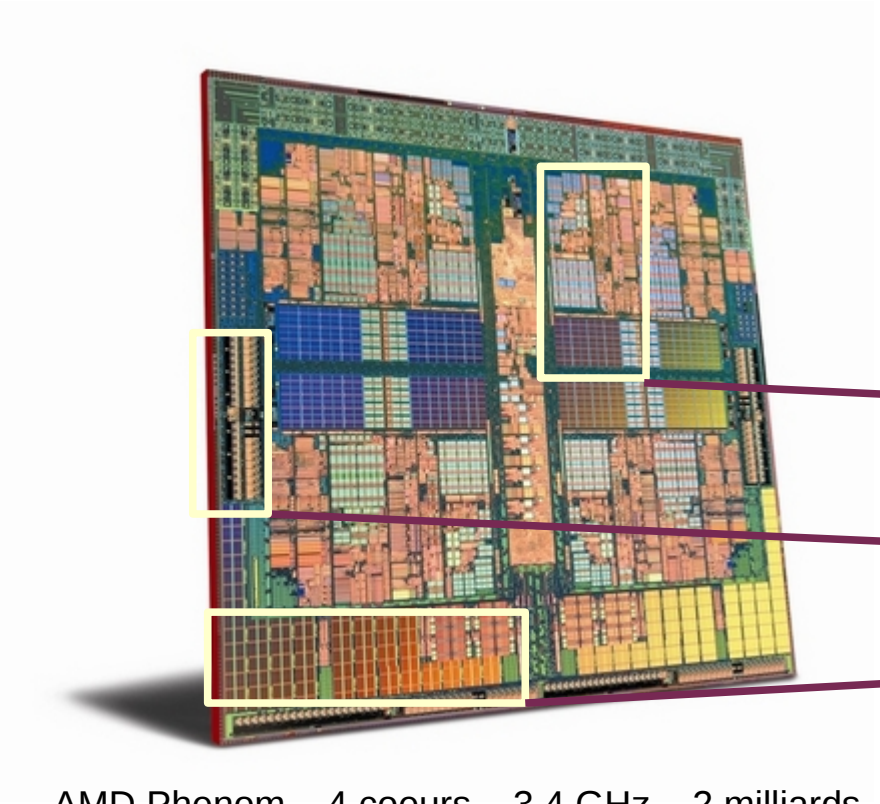
- *Exécution d'**instructions** de **manière séquentielle***
- ***Unités de calculs** précablées*

Plusieurs **coeurs** de calculs identiques

Gestion des **flux** de données

Mémoire **tampon** (ou cache)

Traitement numérique



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- *Exécution d'**instructions** de **manière séquentielle***
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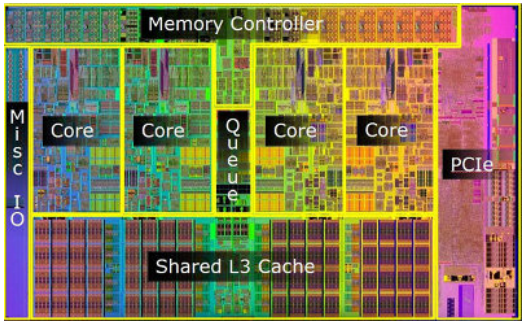

Intel Core i7 (Gulftown) – 4 coeurs - 3.33 GHz – 1.17 milliards

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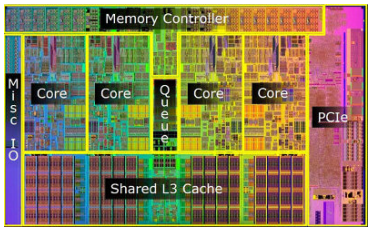
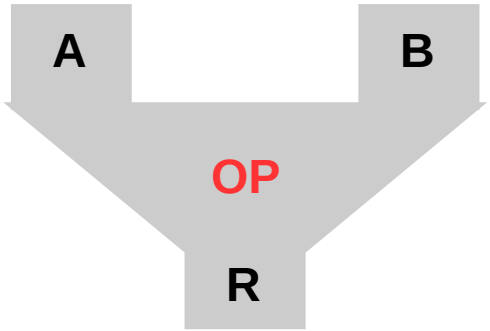
Traitement numérique / Processeur

- **Unité de calculs / Coeur**
  - *Calculs prédéfinis / instructions*
  - *2-3 milliards de calculs à la seconde*



Intel Core i7



Type d'opérations

- *Déplacement de mémoire*
- *Opérations arithmétiques*
- *Opérations logiques*

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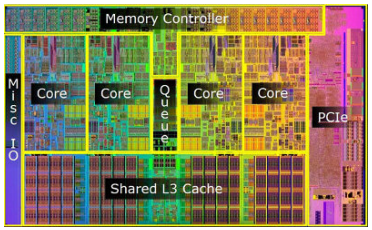
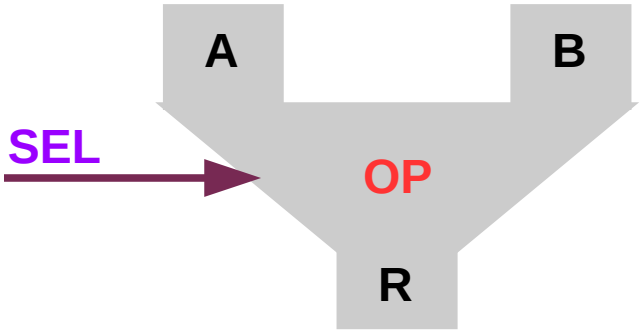
Traitement numérique / Processeur

- **Unité de calculs / Coeur**
  - *Calculs prédéfinis / instructions*
  - *2-3 milliards de calculs à la seconde*



Intel Core i7



Type d'opérations

- *Déplacement de mémoire*
- *Opérations arithmétiques*
- *Opérations logiques*

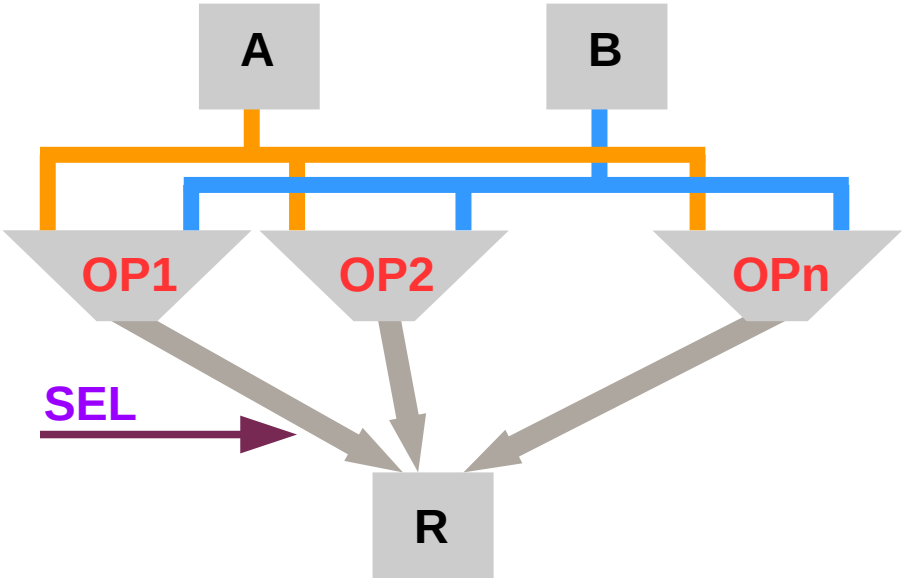
Nombre d'opérations

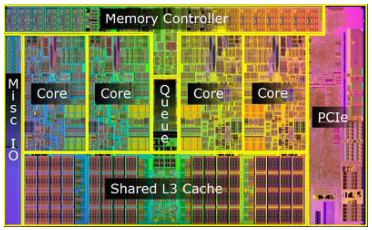
- *Environ 2.000 instructions*

Julien VILLEMEJANE - 1A2S

Traitement numérique / Processeur

- **Unité de calculs / Coeur**
  - *Calculs prédéfinis / instructions*
  - *2-3 milliards de calculs à la seconde*





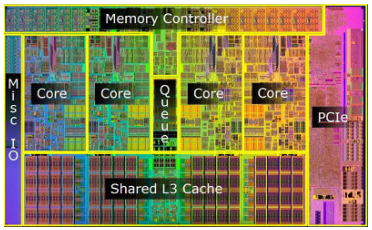
Intel Core i7

Choix de l'opération

- ***Multiplexage***

Traitement numérique / Processeur

- **Instruction**
  - *Décodée par le coeur de calcul*
  - *Définie le type de calcul à réaliser*



Intel Core i7

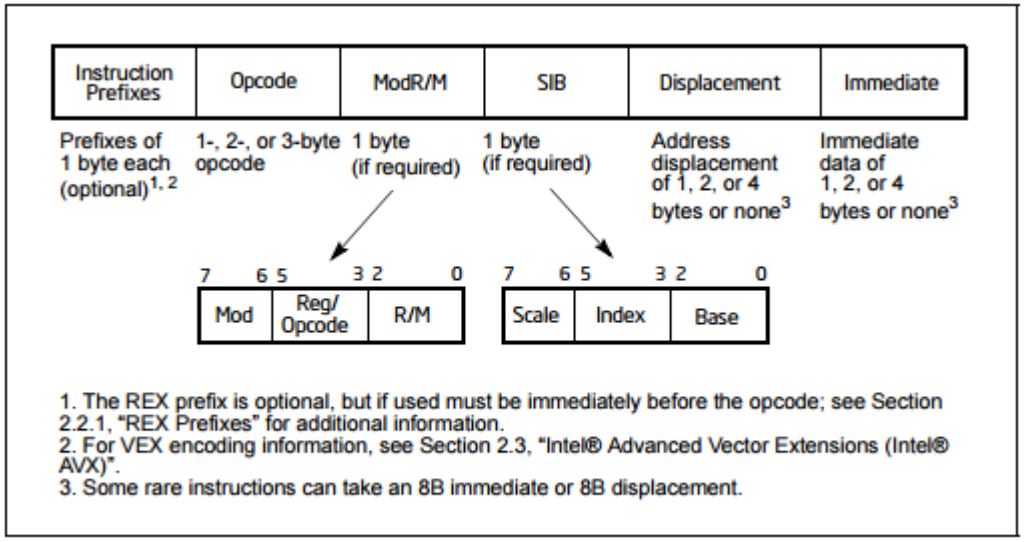


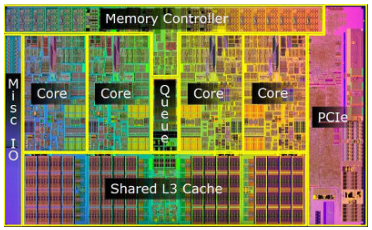
Figure 2-1. Intel 64 and IA-32 Architectures Instruction Format

Choix de l'opération

- ***Multiplexage***
- ***Décodage*** / *OPCODE*

Traitement numérique / Processeur

Instruction / ADDITION



Intel Core i7

ADD—Add

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
04 *ib*	ADD AL, *imm8*	I	Valid	Valid	Add *imm8* to AL.
05 *iw*	ADD AX, *imm16*	I	Valid	Valid	Add *imm16* to AX.
05 *id*	ADD EAX, *imm32*	I	Valid	Valid	Add *imm32* to EAX.
REX.W + 05 *id*	ADD RAX, *imm32*	I	Valid	N.E.	Add *imm32 sign-extended to 64-bits* to RAX.
80 /0 *ib*	ADD *r/m8, imm8*	MI	Valid	Valid	Add *imm8* to *r/m8.*
REX + 80 /0 *ib*	ADD *r/m8**, *imm8*	MI	Valid	N.E.	Add *sign*-extended *imm8* to *r/m64.*

Description

Adds the destination operand (first operand) and the source operand (second operand) and then stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

Operation

DEST ← DEST + SRC;

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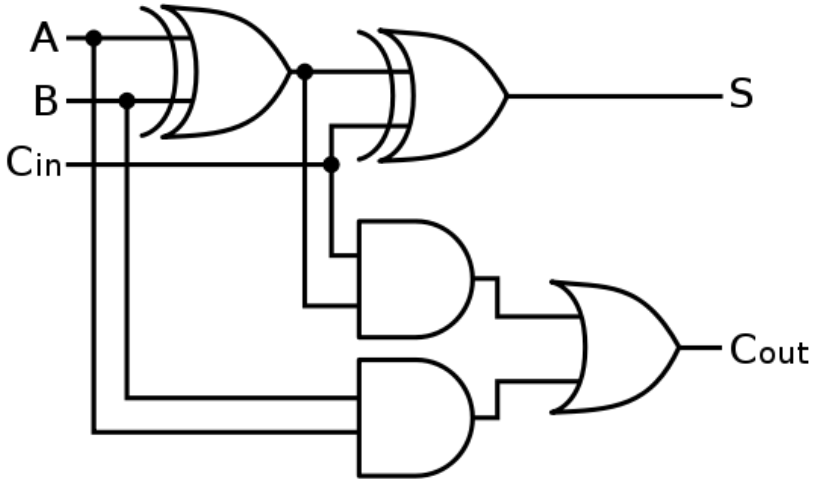
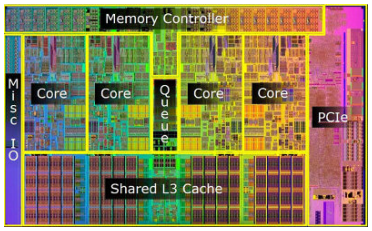
Traitement numérique / Processeur

- **Instruction / ADDITION**
  - *Purement combinatoire – pour 1 bit avec retenue*





Intel Core i7

Opérations

- ***Addition** : combinatoire*

Operation

DEST ← DEST + SRC;

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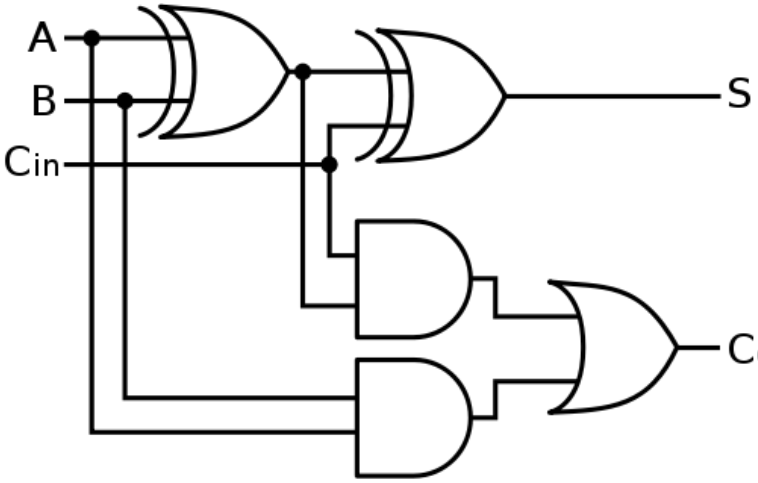
Traitement numérique / Processeur

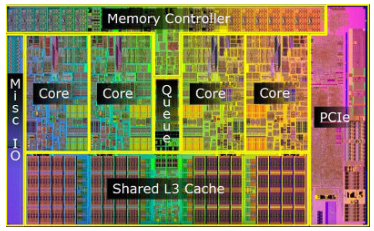
- **Instruction / ADDITION**
  - *Purement combinatoire – pour 1 bit avec retenue*



Operation

DEST ← DEST + SRC;

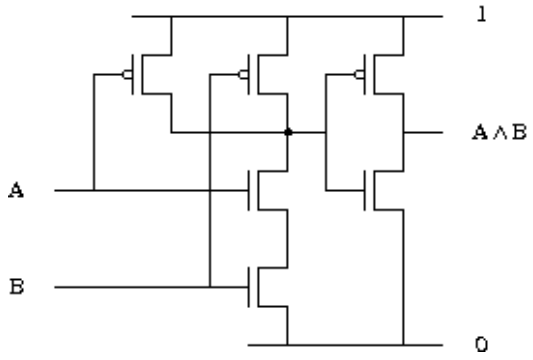
~30 transistors pour 1 bit

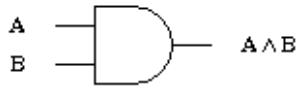


Intel Core i7

Opérations

- ***Addition** : combinatoire*





- ***6 transistors***

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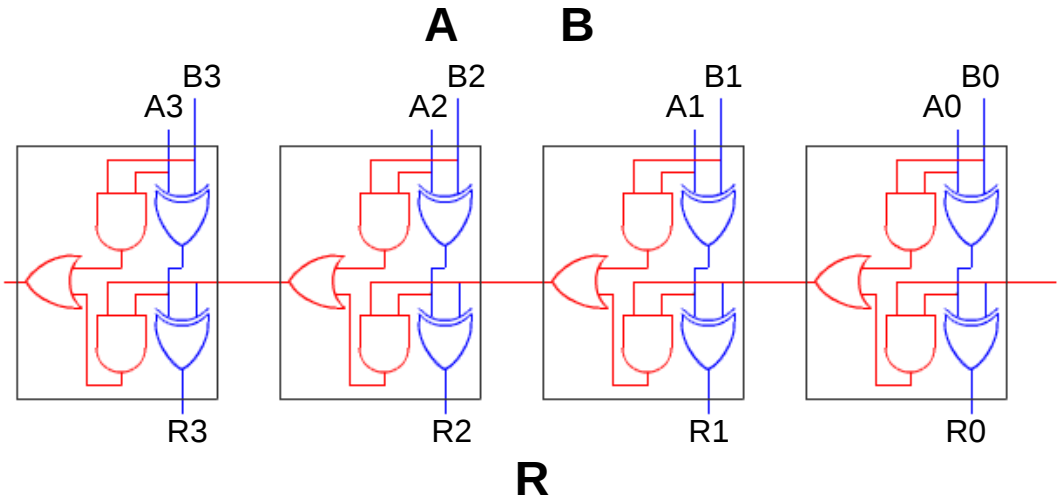
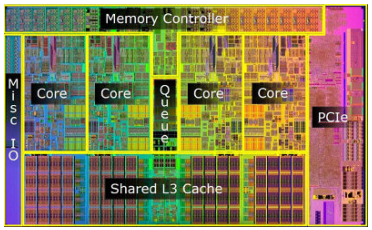
Traitement numérique / Processeur

- **Instruction / ADDITION**
  - *Purement combinatoire – pour n bits avec retenue*





Intel Core i7

Opérations

- ***Addition** : combinatoire*

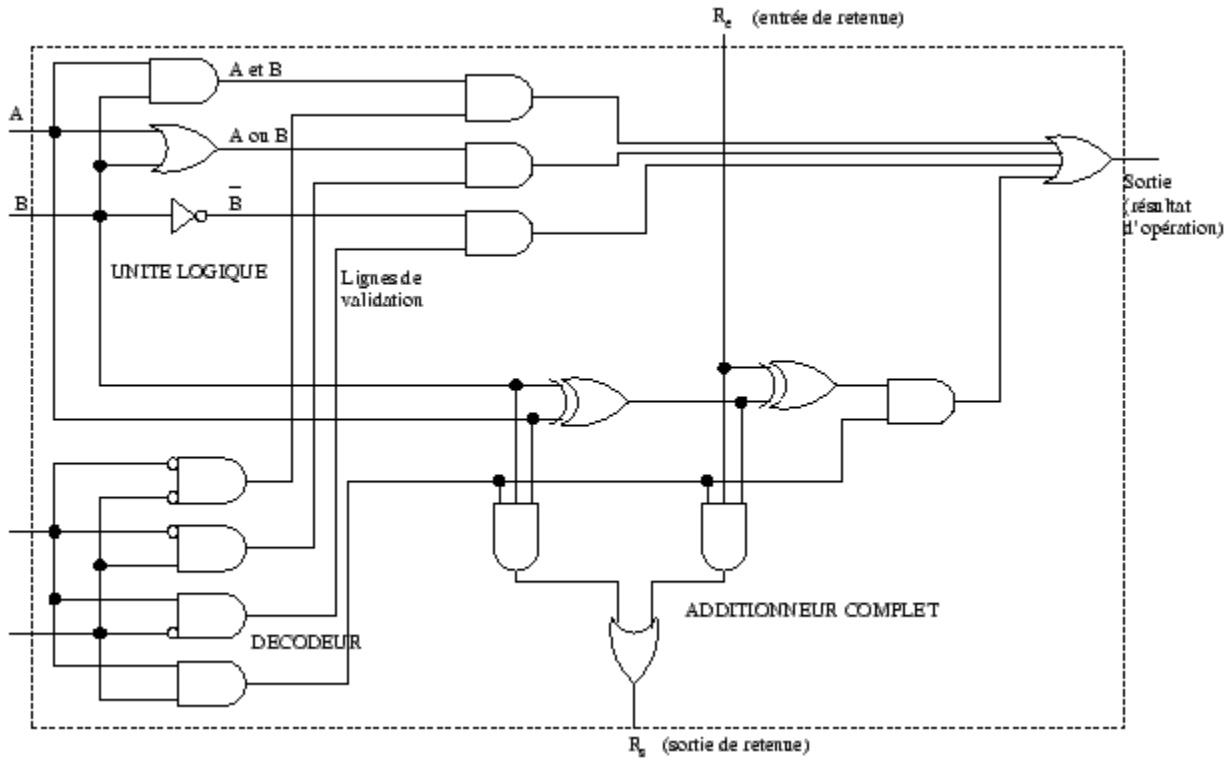
~120 transistors pour 4 bits

Operation

DEST ← DEST + SRC;

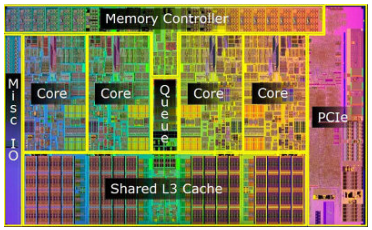
Traitement numérique / Processeur

- **Unité arithmétique et logique / 1 bit – ET/OU/NON/Somme**



Traitement numérique / Processeur

- **Instruction / ADDITION VIRGULE FLOTTANTE**



Intel Core i7

ADDPD—Add Packed Double-Precision Floating-Point Values

Opcode/ Instruction	Op / En	64/32 bit Mode Support	CPUID Feature Flag	Description
66 0F 58 /r ADDPD xmm1, xmm2/m128	RM	V/V	SSE2	Add packed double-precision floating-point values from xmm2/mem to xmm1 and store result in xmm1.
VEX.NDS.128.66.0F.WIG 58 /r VADDPD xmm1,xmm2, xmm3/m128	RVM	V/V	AVX	Add packed double-precision floating-point values from xmm3/mem to xmm2 and store result in xmm1.
VEX.NDS.256.66.0F.WIG 58 /r VADDPD ymm1, ymm2, ymm3/m256	RVM	V/V	AVX	Add packed double-precision floating-point values from ymm3/mem to ymm2 and store result in ymm1.

Description

Add two, four or eight packed double-precision floating-point values from the first source operand to the second source operand, and stores the packed double-precision floating-point results in the destination operand.

- ***Plusieurs unités de calcul différentes***

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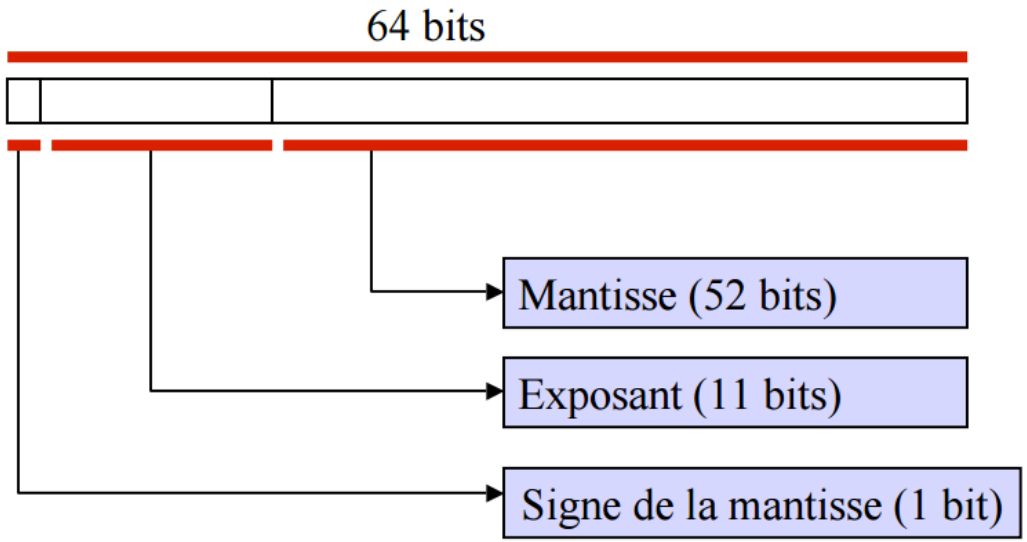
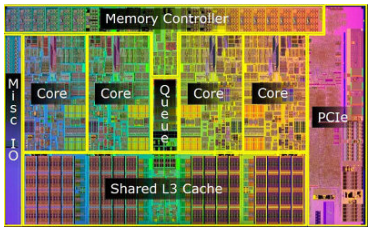
Traitement numérique / Processeur

- **Instruction / ADDITION VIRGULE FLOTTANTE**





Intel Core i7

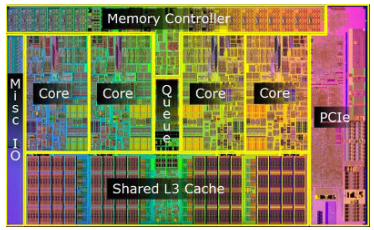
Norme IEEE 754

$$X = \pm 1,M \cdot 2^{e}$$

- ***Plusieurs unités de calcul différentes***

Traitement numérique / Processeur

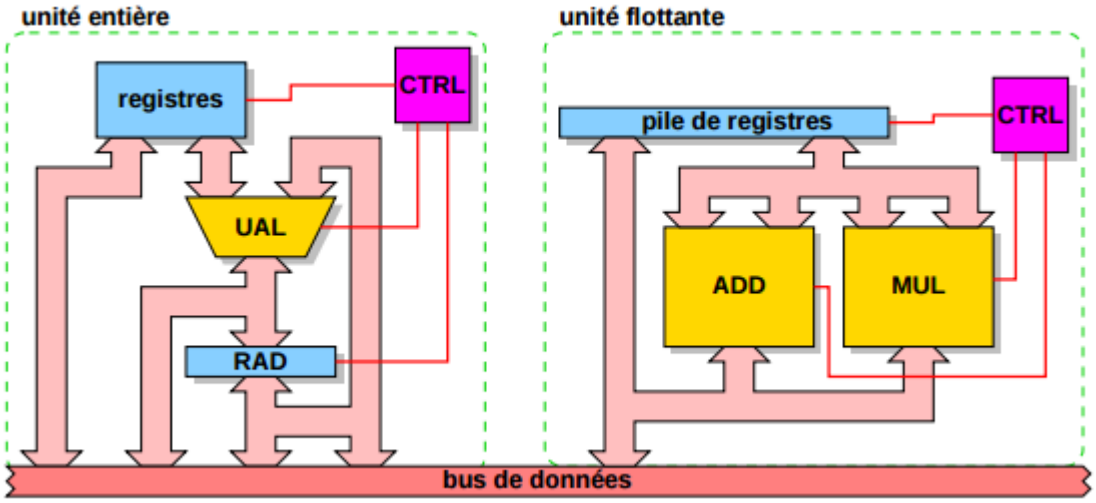
- **Instruction / CONVERSION**



Intel Core i7

CVTDQ2PD—Convert Packed Doubleword Integers to Packed Double-Precision Floating-Point Values

Opcode/ Instruction	Op / En	64/32 bit Mode Support	CPUID Feature Flag	Description
F3 0F E6 /r CVTDQ2PD xmm1, xmm2/m64	RM	V/V	SSE2	Convert two packed signed doubleword integers from xmm2/mem to two packed double-precision floating-point values in xmm1.



A. TISSERAND / LIRMM

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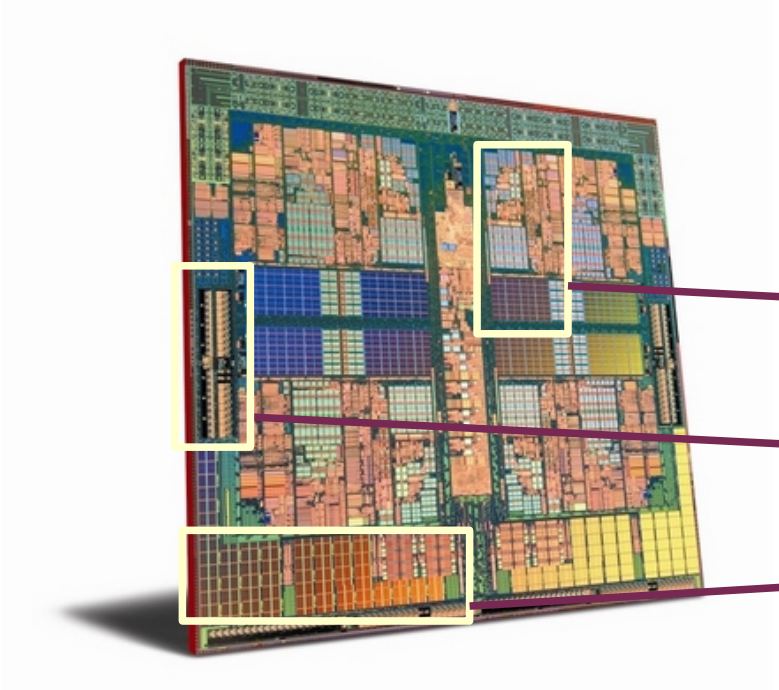
Traitement numérique / Processeur

- **Unité de calculs séquentiels**
  - *2-3 milliards de calculs à la seconde*



AMD Phenom – 4 coeurs – 3.4 GHz – 2 milliards

Séquenceur

- ***Compteur** d'adresse*

Plusieurs **coeurs** de calculs identiques

Gestion des **flux** de données

Mémoire **tampon** (ou cache)

25 Go/s

Julien VILLEMEJANE - 1A2S

De plus en plus de données à traiter...

Caméra 2K – stéréo

- *2048 x 1080 pixels*
- *60 images par seconde / fps*
- *24 bits / pixels = 3 octets*

~ 400 Mo / s / image

Traitement en parallèle

De plus en plus de données à traiter...

Caméra 2K – stéréo

- *2048 x 1080 pixels*
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- *24 bits / pixels = 3 octets*

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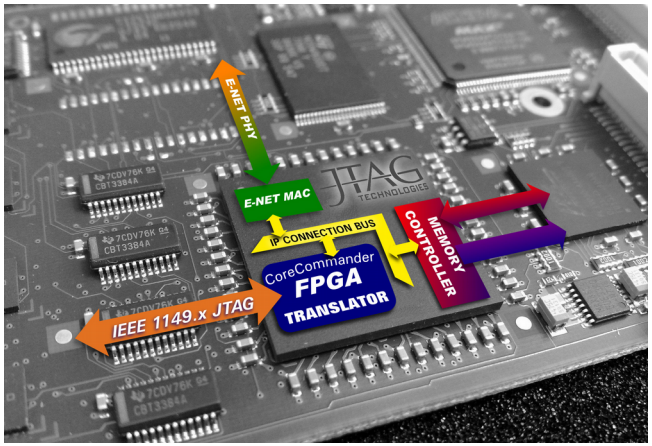
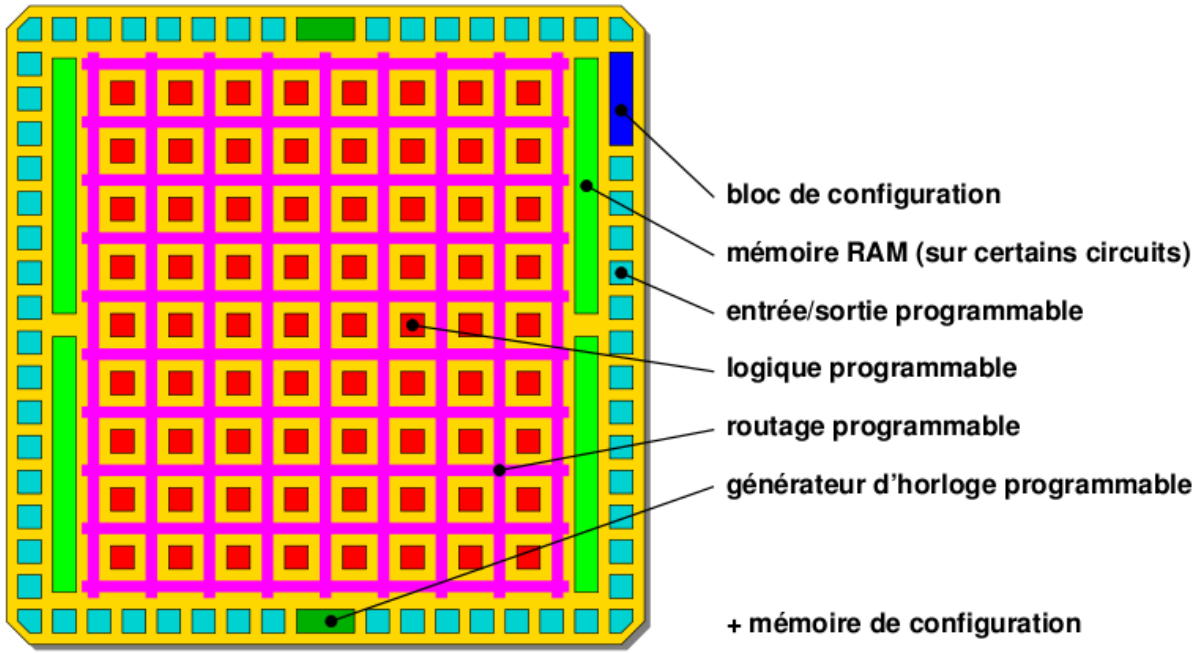
Traitement en parallèle



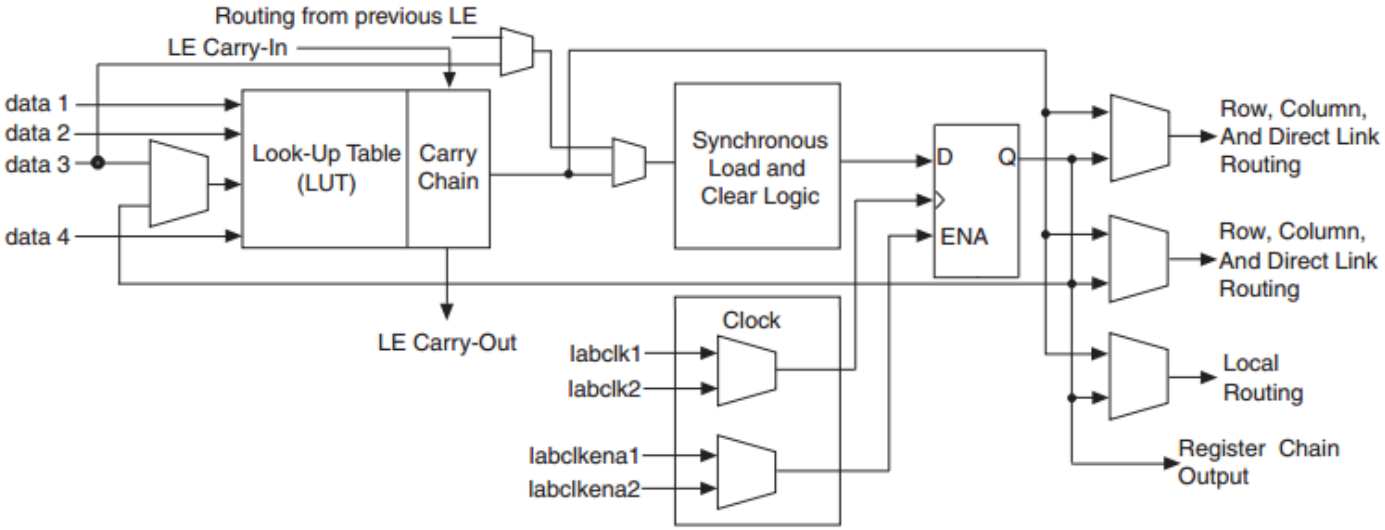
FPGA

- **Field Programmable Gate Array**
  - *Interconnexion de composants logiques*

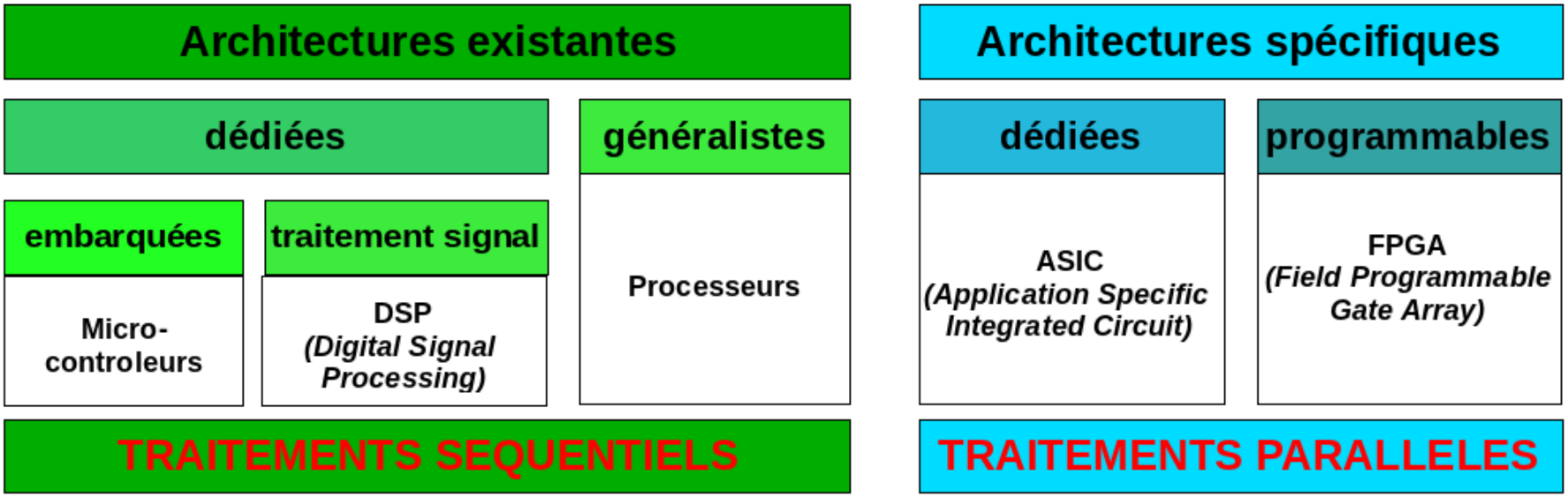


FPGA

- **Field Programmable Gate Array**
  - *Interconnexion de composants logiques*
  - *Combinatoire (LUT) / Séquentiel*

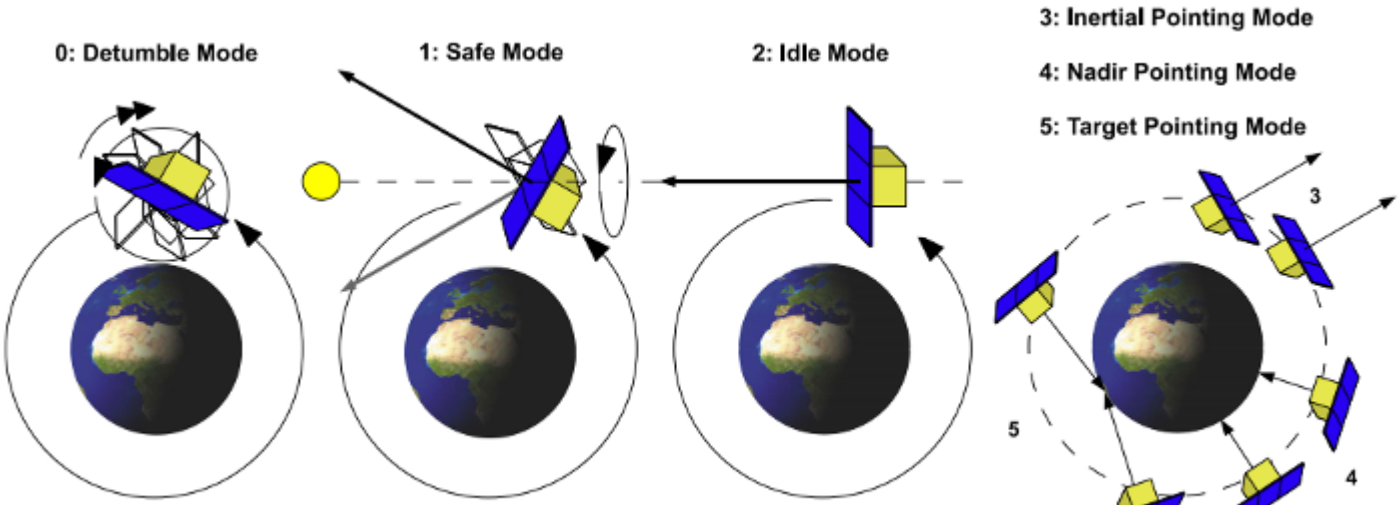


Systèmes numériques / Classification



FPGA

- **Field Programmable Gate Array**
  - *Premières applications dans le spatial et le militaire*



Attitude control modes of ACS

From 'Toshinori Kuwahara' thesis - Japan - 2009

FPGA

- **Field Programmable Gate Array**
  - ➔ *Parallélisation des calculs*

Sensors

Ensuring Reliable Networks TTTech

Bordeaux

FPGA

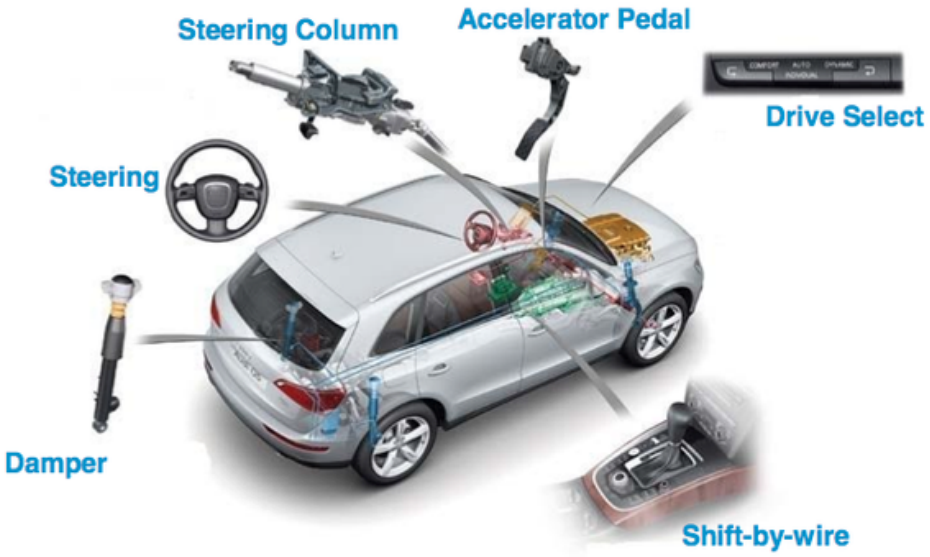
- **Field Programmable Gate Array**
  - ➔ *Parallélisation des calculs*

Audi

Actuators

Ensuring Reliable Networks TTTech

Necessary Actuators for Automated Driving	
▸ Electronic Stability Control	▸ Powertrain Coordination
▸ Hold management system	▸ Shift-by-Wire
▸ Decelleration management	▸ Electric Power Steering



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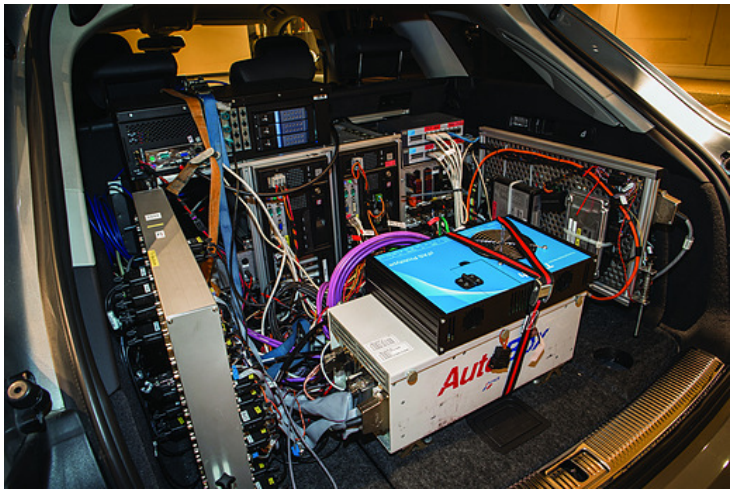
FPGA

- **Field Programmable Gate Array**
  - *Parallélisation des calculs*



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FPGA

- **Field Programmable Gate Array**
  - *Parallélisation des calculs*

Altera: Automotive Vision System Design Variables and FPGA Advantages

Design Challenges	System Variables	FPGA Advantages
Data acquisition	Different camera sensor resolutions, frame rates; different types of sensors required (radar, laser, video). No standard way to communicate data into car network.	Customized sensor interfaces and intellectual property (IP) cores to enable connectivity to any automotive network standard.
Data processing	Varying image processing algorithms for image correction and video analytics. Stitching multiple camera data into a 360° image. Fusing multiple types of sensor data. Real-time processing requirements.	Ability to implement customized algorithms in hardware and software for video and image processing.
Communications	Different communication standards for audio/video data, such as media-oriented system transport (MOST), Ethernet, and LVDS. Need to connect all systems together in a single low-cost system bus.	Ability to design the exact type and number of communications interfaces needed for your advanced driver assistance systems (ADAS) application.

Systèmes numériques / Avantages-Inconvénients

Architectures existantes

- **Large choix de composants**
- **Modules déjà existants**
  - *ADC, PWM, Timers, Communication*
- **Gestion de l'horloge**
- **Facilité de mise en oeuvre**

- **Execution séquentielle des calculs**
- **Instructions prédéfinies**
- **Utilisation réservée de certains modules**

Architectures spécifiques

- **Très grande densité**
- **Grand nombre d'E/S**
- **Exécution parallélisable**
- **Gestion d'horloge avancée**
- **Reconfiguration dynamique**

- **Volatiles (cellules RAM)**
- **Circuits imprimés multicouches**
- **Aucun module précablé**
- **Entrées-sorties numériques**

FPGA

- **Nouveautés**

This will allow FPGA users to utilize the high bandwidth and compact size advantages of parallel optical interfaces that are currently used in data centers.

Philip Gadd, *vice president and general manager of the Fiber Optics Product Division at Avago*

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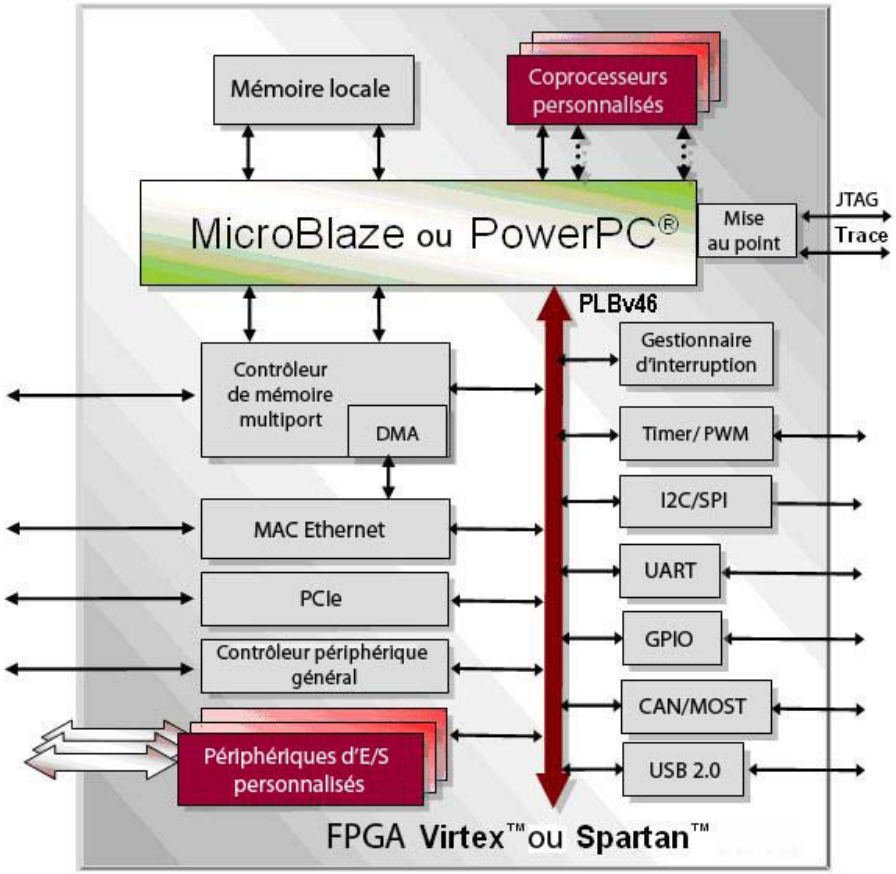
FPGA

- **Nouveautés**

XILINX®

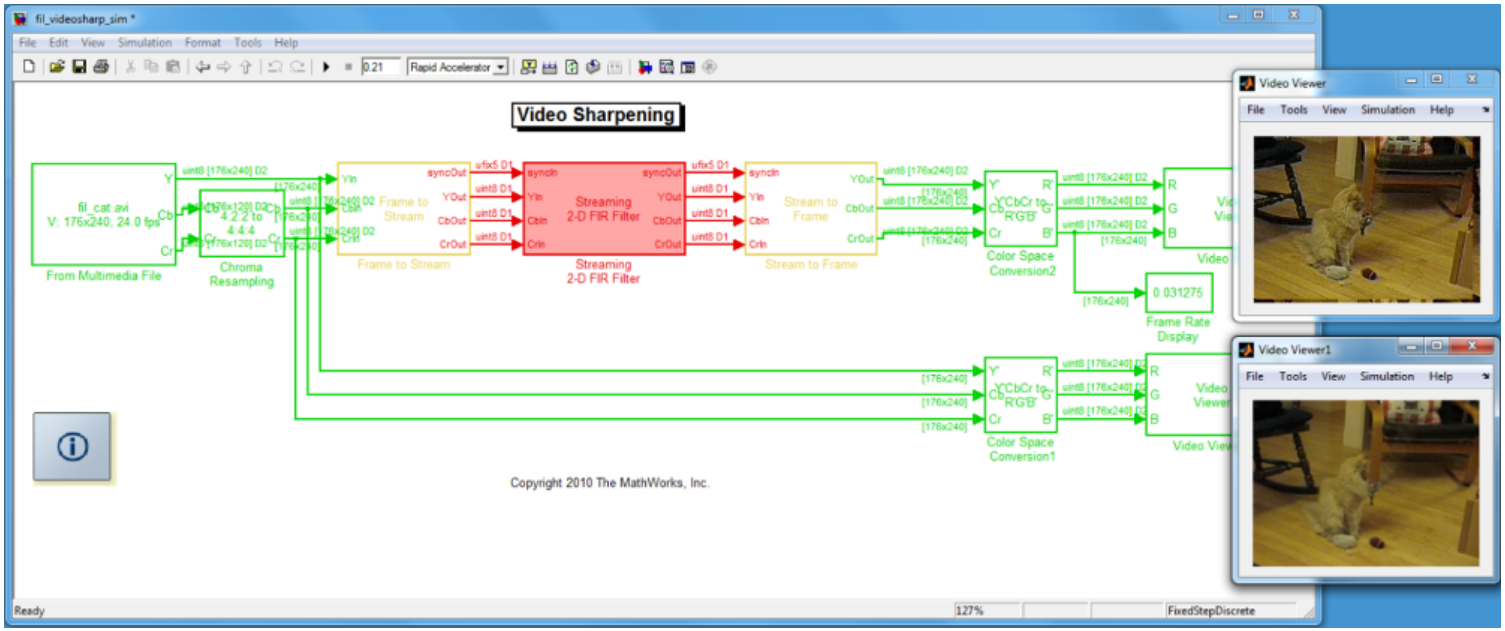


FPGA

- **Nouveautés**

MathWorks

NATIONAL INSTRUMENTS LabVIEW



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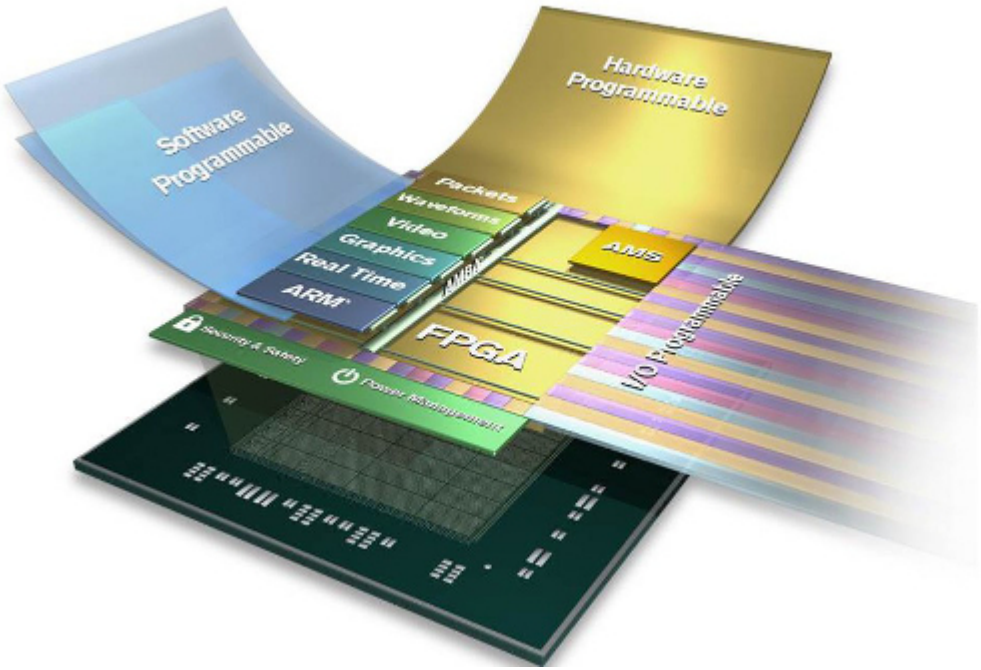
FPGA + uC = SoC



Architectures spécifiques

- Très grande densité
- Grand nombre d'E/S
- Exécution parallélisable
- Gestion d'horloge avancée
- Reconfiguration dynamique

- Aucun module précablé
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- Volatiles (cellules RAM)
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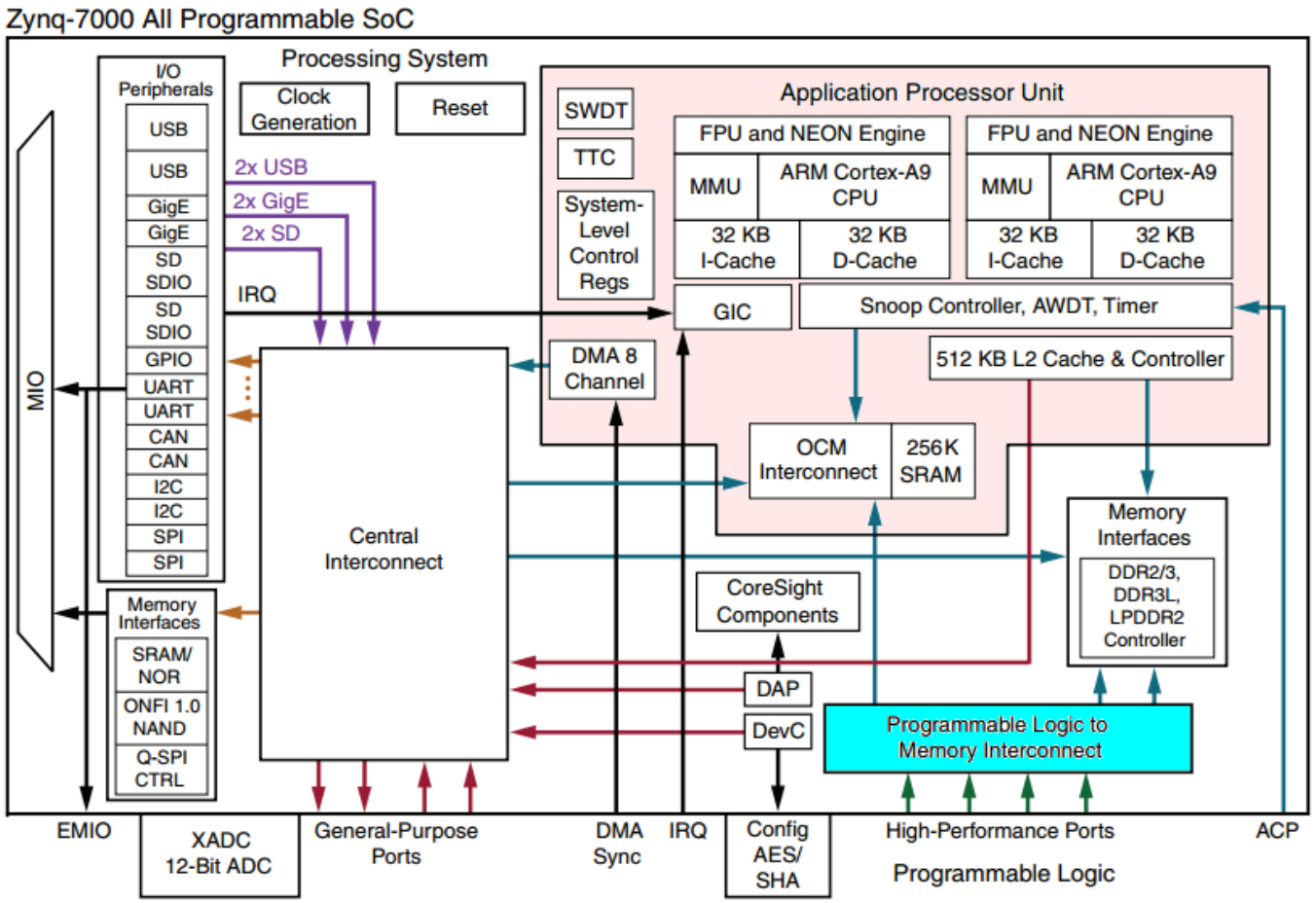
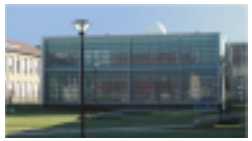
FPGA + uC = SoC

XILINX




Paris-Saclay


Saint-Étienne

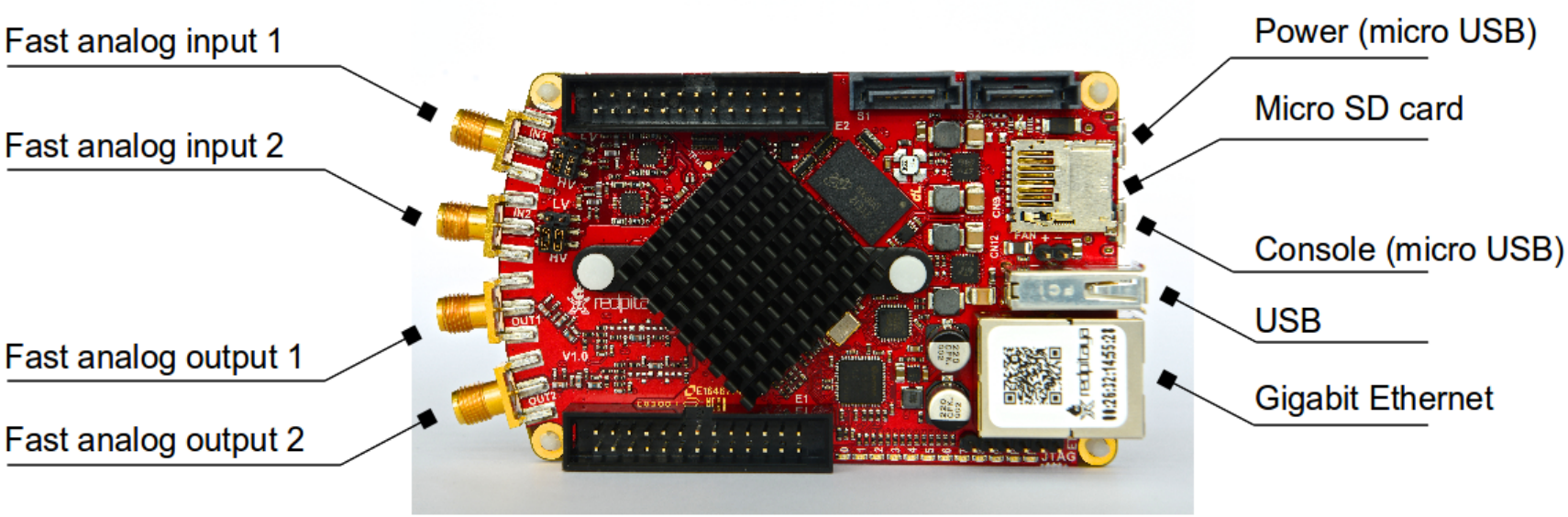

Bordeaux

Nouvelles cartes de prototypage / Mixte

redpitaya

125 Mech/s

300 €



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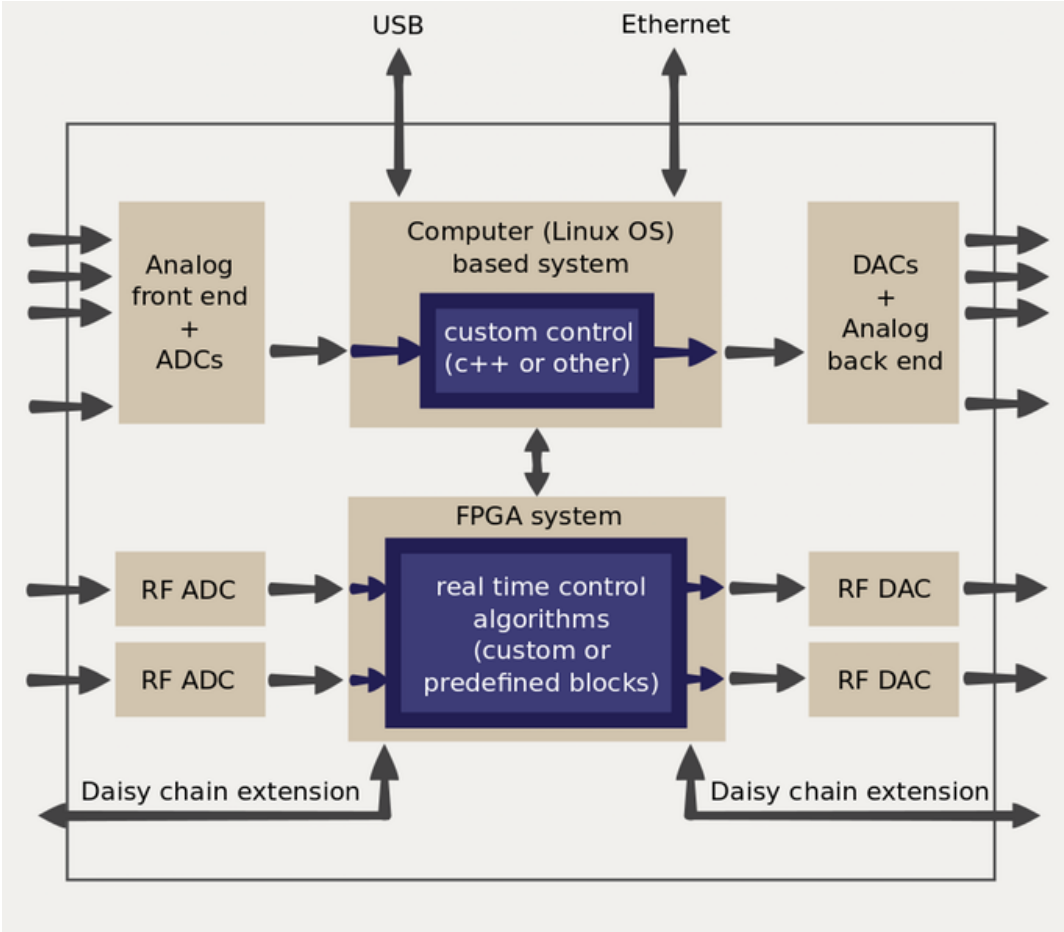
Nouvelles cartes de prototypage / Mixte

redpitaya

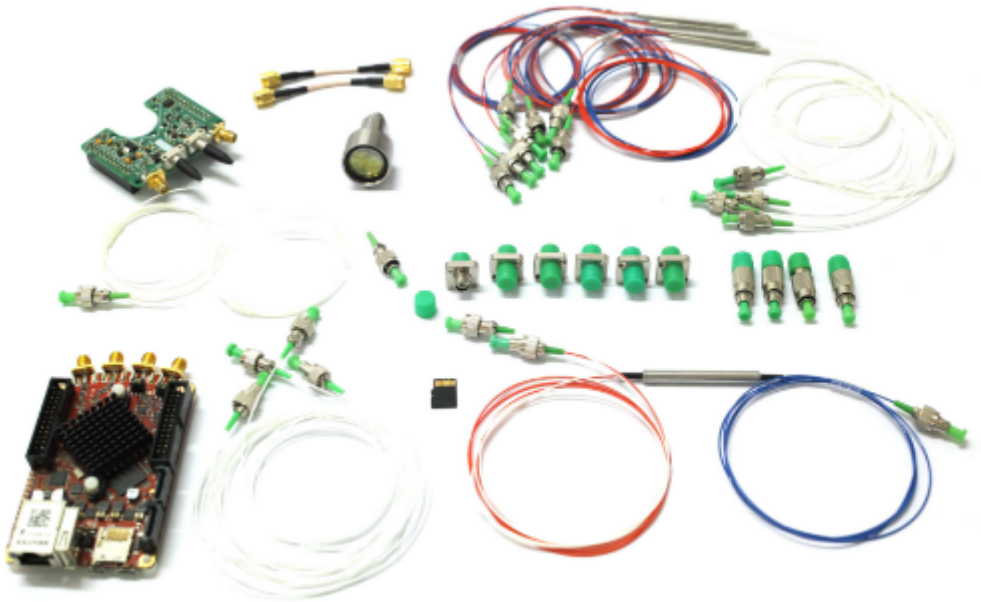


Nouvelles cartes de prototypage / Mixte

Koheron

Laser development kit

Learn photonics and develop fibered sensing systems



LDK

- 1550 nm DFB laser (eye-safe)
- 60 MHz modulation / detection
- Web-based interface
- RedPitaya oscilloscope (optional)
- Python, C / C++ API
- FPGA / Linux SDK

Standard: 695 €

Extended: 1345 €

Request a quote

Julien VILLEMEJANE - 1A2S

Nouvelles cartes de prototypage / Mixte

Koheron

150 MHz low-noise photodetection

Amplified photodetection for coherent sensing

PD100

- 900 - 1700 nm operation (InGaAs)
- 150 MHz bandwidth at 3 dB
- AC coupled
- 3900 V/A transimpedance gain

295 €

Request a quote

Des EB de données à traiter

CISCO

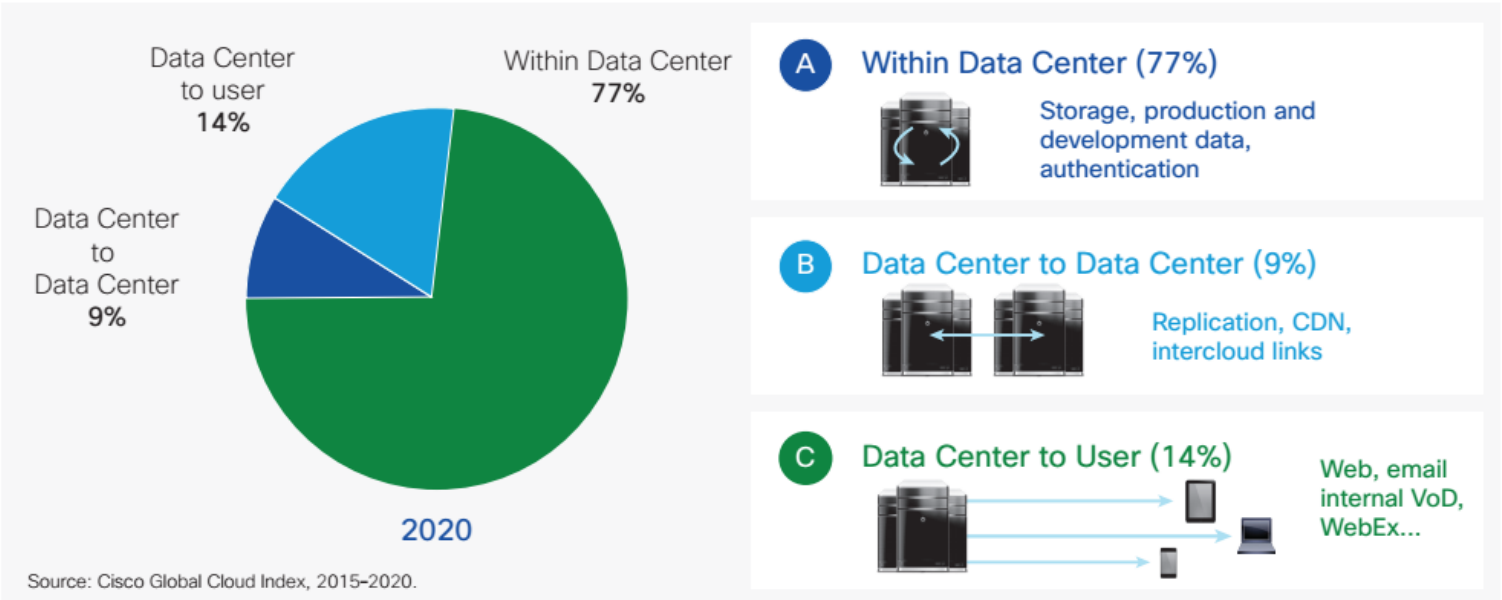
Data Center IP Traffic, 2015–2020	2015	2016	2017	2018	2019	2020	CAGR 2015–2020
By Type (EB per Year)							
Data center to user	744	933	1,164	1,438	1,772	2,183	24.0%
Data center to data center	346	515	713	924	1,141	1,381	31.9%
Within data center	3,587	5,074	6,728	8,391	10,016	11,770	26.8%
By Segment (EB per Year)							
Consumer	2,997	4,304	5,836	7,435	9,075	10,906	29.5%
Business	1,681	2,218	2,768	3,318	3,853	4,429	21.4%
By Type (EB per Year)							
Cloud data center	3,851	5,636	7,712	9,802	11,850	14,076	29.6%
Traditional data center	827	885	892	951	1,078	1,259	8.8%
Total (EB per Year)							
Total data center traffic	4,678	6,522	8,604	10,753	12,928	15,335	26.8%

TB : TeraOctets 10^{12} ,
PB : PetaOctets 10^{15} ,
EB : ExaOctets 10^{18}

Des EB de données à traiter

CISCO

Figure 5. Global Data Center Traffic by Destination in 2020



Source: Cisco Global Cloud Index, 2015–2020.

TB : TeraOctets 10^{12} ,
PB : PetaOctets 10^{15} ,
EB : ExaOctets 10^{18}

Julien VILLEMEJANE - 1A2S

Des EB de données à traiter

Figure 26. Smart City: Multiple Applications Create Big Data

TB : TeraOctets 10^{12} ,
PB : PetaOctets 10^{15} ,
EB : ExaOctets 10^{18}

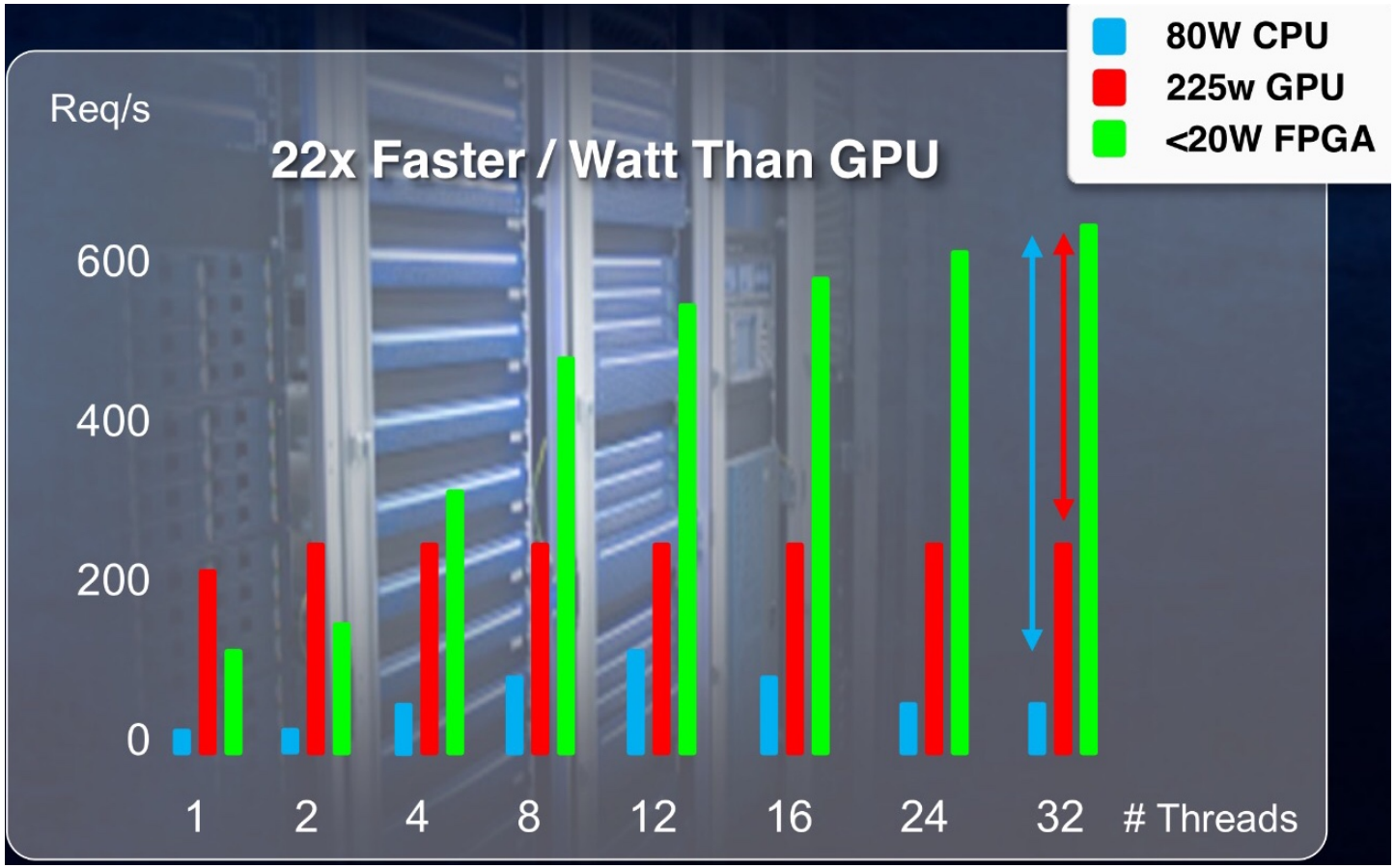
FPGA / Numérique

Intel sees FPGAs as the key to designing a new generation of products to address emerging customer workloads.

CLICK TO TWEET

"We think FPGAs are very strategic," said Raejeanne Skillern, GM of the Cloud Service Provider Business at Intel. "We're doing a lot of development with OEMs and customers, and continuing to implement (FPGAs) into our roadmap."

FPGA / Numérique



2014/12 - Gazettabyte.com

FPGA / Numérique

amazon web services

30 novembre 2016